Amendments to the Claims

The following Listing of Claims replaces all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (currently amended): A common carrier, comprising:

a carrier substrate having an upper surface; and

a plurality of integrated chips distributed across the carrier substrate, each integrated chip including a respective substrate supporting an integrated structure; and

a plurality of adhesive bonds each adhering a respective integrated chip to the carrier substrate;

wherein alignment between the integrated chip substrates is within a first alignment tolerance range and alignment between the integrated structures supported by the integrated chip substrates is within a second alignment tolerance range smaller than the first alignment tolerance range ~~adhered on the upper surface and aligned with each other with lithographic alignment tolerance~~.

Claim 2 (currently amended): The common carrier as described in Claim 1, wherein the adhesive bonds comprise an adhesive material selected from polysilicon, glass, metal, and ceramic ~~unprocessed integrateable form of the integrated chips are adhered to the carrier substrate using an adhesive which retains adherence reliability when exposed to subsequent processing steps performed on the common carrier~~.

Claim 3 (currently amended): The common carrier as described in Claim 1, wherein the carrier substrate, the adhesive bonds, and the integrated chips have essentially the same coefficient of thermal expansion (CTE).

Claim 4 (currently amended): The common carrier as described in Claim 1, wherein the carrier substrate comprises one of polysilicon, glass, metal, and ceramic.

Claim 5 (currently amended): The common carrier as described in Claim 1, wherein the carrier substrate includes a plurality of slots each containing a respective integrated chip ~~for adhering the plurality of chips, one chip per slot~~.

Claim 6 (currently amended): The common carrier as described in Claim 5, wherein the upper surface of the carrier substrate and upper surfaces of the integrated chips are substantially coplanar ~~each have parallel top surfaces which reside essentially with the same plane~~.

Claim 7 (currently amended): The common carrier as described in Claim 6, wherein the upper surface of the carrier substrate and the upper surfaces ~~unprocessed, integrateable form~~ of the integrated chips are polished ~~prior to being lithographically processed~~.

Claim 8 (currently amended): The common carrier as described in Claim 1, wherein the adhesive bonds adhere respective substrates of ~~the carrier substrate and~~ the integrated chips to the upper surface of the carrier substrate ~~each have parallel top surfaces which do not reside within the same plane~~.

Claim 9 (currently amended): The common carrier as described in Claim 8, wherein the integrated structures of the integrated chips are substantially non-coplanar with the upper surface of the carrier substrate ~~unprocessed, integrateable chip form of the plurality of chips is lithographically processed using a curtain coating photoresist deposition~~.

Claim 10 (currently amended): The common carrier as described in Claim [[7]] 5, further comprising [[a]] filler material disposed in each ~~adapted to fill a~~ peripheral gap between [[the]] interior edges of each slot and ~~of the slots and the~~ peripheral edges of each respectively contained integrated chip ~~of the unprocessed, integrateable form of the integrated chips when each chip is adhered within each slot and prior to being polished~~.

Claim 11 (currently amended): The common carrier as described in Claim [[9]] 10, wherein the filler material comprises glass frit.

Claim 12 (currently amended): The common carrier as described in Claim 1, wherein the integrated structure of each integrated chip comprises an electrically conductive node, and further comprising ~~: at least two electrically conductive nodes, the electrically conductive nodes are disposed on either one of the chip and the carrier substrate; and~~ an interconnect ~~adapted to~~ electrically connecting [[connect the]] electrically conductive nodes of the integrated chips.

Claim 13 (currently amended): The common carrier as described in Claim 1, wherein each of the plurality of integrated chips is a component ~~selected from a group consisting~~ of a respective [[an]] inkjet printhead ~~, a thermal inkjet printhead, a semiconductor, an integrated circuit, an ASIC, a MicroElectroMechanical System, and a fluidic device~~.

Claim 14 (withdrawn): A method of forming a common carrier comprising the steps of:

adhering an unprocessed, integrateable form of a plurality of chips on the upper surface of a carrier substrate according to a first placement alignment precision;

lithographically processing the unprocessed, integrateable form of the plurality of chips to form a plurality of integrated chips on the upper surface, wherein the integrated chips are aligned with each other and the substrate with a second alignment precision having lithographic processing tolerances.

Claim 15 (withdrawn): The method of forming the common carrier as described in Claim 14 wherein the first alignment precision has a greater tolerance range than the lithographic processing tolerances.

Claim 16 (withdrawn): The method of forming the common carrier as described in Claim 14 wherein the first alignment precision has a tolerance in the range of +/- 1 milimeter and the second alignment precision has a tolerance in the range of less than 1 micron.

Claim 17 (withdrawn): The method of forming the common carrier as described in Claim 14 further comprising the steps of:

forming a plurality of slots within the upper surface of the carrier substrate according to the first alignment precision; and

adhering the unprocessed, integrateable form of the integrated chips within the plurality of slots.

Claim 18 (withdrawn): The method of forming the common carrier as described in Claims 17 further comprising the step of depositing a filler so as to fill a peripheral gap between the interior edges of each of the slots and the peripheral edges of each of the unprocessed, integrateable form of the integrated chips when each unprocessed chip is adhered within each slot.

Claim 19 (withdrawn): The method of forming the common carrier as described in Claim 18 further comprising the step of polishing the upper surface of the plurality of chips to be in essentially the same parallel plane as the upper surface of the carrier substrate.

Claim 20 (withdrawn): The method of forming the common carrier as described in Claim 14 further comprising the step of adhering the unprocessed, integrateable form of the integrated chips directly on the upper surface of the carrier substrate such that the upper surface of the unprocessed, integrateable chips is in a parallel, but different, plane than the upper surface of the substrate carrier.

Claim 21 (withdrawn): The method of forming the common carrier as described in Claim 20 further comprising the step of lithographically processing using curtain coating deposition.

Claim 22 (new): The common carrier as described in Claim 1, wherein the first alignment tolerance range corresponds to a semiconductor chip placement tool alignment tolerance range and the second alignment tolerance range corresponds to a semiconductor lithographic process alignment tolerance range.

Claim 23 (new): The common carrier as described in Claim 1, wherein the first alignment tolerance range is ± 1 millimeter, and the second alignment tolerance range is smaller than 1 micrometer.

Claim 24 (new): The common carrier as described in Claim 5, wherein alignment between the slots of the carrier substrate is within the first alignment tolerance range.

Claim 25 (new): The common carrier as described in Claim 10, wherein the filler material in each gap has a polished upper surface substantially coplanar with the upper surface of the carrier substrate.